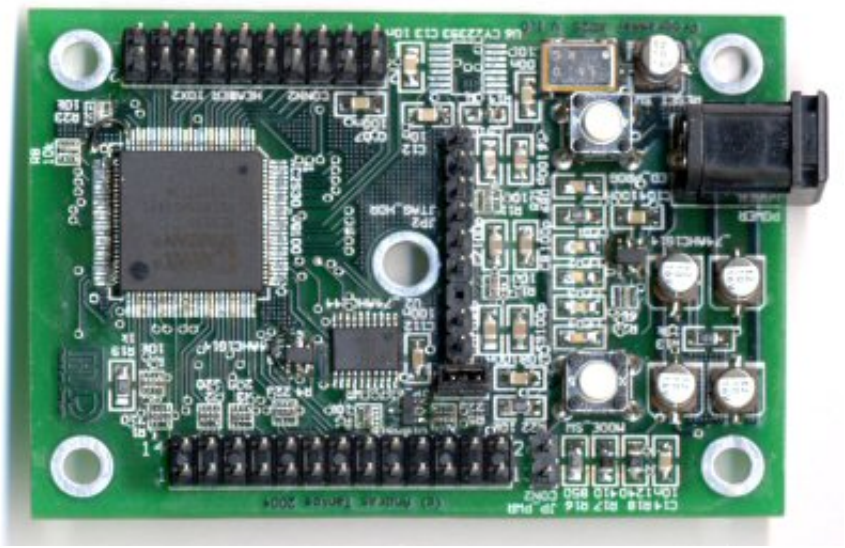
Parallel port JTAG programmer 2

Author : Andras Tantos



Introduction

This project is similar to the CPLD-based programmer in many ways. It also connects to the parallel port of the PC and it also allows for the emulation of many different JTAG devices. While the other device uses a CPLD with non-volatile configuration and a limited number of reprogramming options, this one uses an FPGA for the same purpose. The FPGA can be reconfigured as many times as needed, in fact it needs to be reconfigured after every power-on.

In many cases JTAG programmer, while implementing very similar functionality, vary from vendor to vendor in circuit details. If you use multiple devices with JTAG interfaces from different vendors, let's say a Xilinx FPGA and an ARM7 CPU, you will find yourself constantly changing the JTAG programming device during your development interations. One of the many benefits of an FPGA based JTAG programmer is that it can be configured and re-configured as many times as needed and it can be done fast.

On the to of being a useful universal programming POD, the circuit can also be used as a small development board for FPGA-based projects. The design also incorporates many additinal amenities that make it a versatile development platform and the use of an FPGA instead of a CPLD allows for much more complex designs.

Features

- Printer-port interface
- Integrated 3.3V and 2.5V power supply
- Can provide (3.3V) power for target devices

- Built around a second generation Xilinx Spartan device
- PLL clock generator can provide wide range of operating frequencies
- Multiple different clock sources are available
- Four user-programmable LED and one user-programmable push-button is provided
- 16 GPIO pins are available on the top of the 6 JTAG connector pins

License

This document and all the accompanying design documentation (for example schematic and PCB files) are covered by the H-Storm Non-Commercial License (HSNCL).

H-Storm Non-Commercial License (HSNCL)

Redistribution and use in source or binary forms, or incorporated into a physical (hardware) product, with or without modification, are permitted **for non-commercial use only**, provided that the following conditions are met:

- **The redistribution doesn't result in financial gain.**
- Redistributions of source code must retain the above copyright notice, this list of conditions and the following disclaimer.
- Redistributions in any other form must contain in printed or electronical format the above copyright notice, this list of conditions and the following disclaimer in the documentation and/or other materials provided with the distribution.
- All advertising materials mentioning features or use of this technology must display the following acknowledgment:
  This product includes H-Storm technology developed by Andras Tantos and Modular Circuits.
- Neither the name of Andras Tantos or Modular Circuits may be used to endorse or promote products derived from or using this technology without specific prior written permission.

ALL THE INFORMATION, TECHNOLOGY, AND SOFTWARE IS PROVIDED BY THE AUTHORS ``AS IS'' AND ANY EXPRESS OR IMPLIED WARRANTIES, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE ARE DISCLAIMED. IN NO EVENT SHALL ANDRAS TANTOS, MODULAR CIRCUITS OR CONTRIBUTORS BE LIABLE FOR ANY DIRECT, INDIRECT, INCIDENTAL, SPECIAL, EXEMPLARY, OR CONSEQUENTIAL DAMAGES (INCLUDING, BUT NOT LIMITED TO, PROCUREMENT OF SUBSTITUTE GOODS OR SERVICES; LOSS OF USE, DATA, OR PROFITS; OR BUSINESS INTERRUPTION) HOWEVER CAUSED AND ON ANY THEORY OF LIABILITY, WHETHER IN CONTRACT, STRICT LIABILITY, OR TORT (INCLUDING NEGLIGENCE OR OTHERWISE) ARISING IN ANY WAY OUT OF THE USE OF THIS SOFTWARE OR TECHNOLOGY, EVEN IF ADVISED OF THE POSSIBILITY OF SUCH DAMAGE.

Design description

FPGA

The circuit is centered around the Xilinx XC2S30 FPGA. This device has about 30,000 usable gates, and was the first low-cost FPGA from Xilinx to include embedded SRAM modules. The device also contains versatile clock-management functions and four different clock domains. While the silicon can handle many different I/O standards, the board doesn't provide the required I/O power supplies for many of those. Only the ones that are operational with the standard 3.3V I/O voltage are usable in the design.

The FPGA is hooked up to the printer port on one side and to the JTAG and GPIO pins on the other. For FPGA pins are connected to four LEDs and one push-button to provide user interaction.

FPGA Programming

Upon powerup the FPGA needs to be configured by the host (in this case the PC). The printer port pins and the programming configuration options on the FPGA are set up for the 'parallel slave' configuration mode. This allows very fast download of the programming data since even though the PC must use bit-banging for accessing the chip, data is pushed out one byte at a time. Typical programming file sizes are in the 40kBytes range for this FPGA. A download utility is prodived that can program the FPGA.

JTAG interface to the FPGA

While the initial configuration of the FPGA has to be done in the slave-parallel configuration mode, after the configuration is downloaded, the the parallel port can be turned into a JTAG interface to the FPGA itself. In this mode the board simulates a Xilinx parallel cable III-type programmer attached to the XC2S30 FPGA. Part of this functionality is implemented by U2, part of it however has to be programmed into the FPGA itself. In particular, the FPGA have to pull the JTAG_MODE signal (pin 55) low to direct the parallel port signals to the JTAG pins and it has to connect the PP_DATA6 (pin 56) signal to PP_WAIT (pin 74) and PP_I2 (pin 52) for programmer auto-detect. This mode of operation is useful for debugging: after the configuration is downloaded, the parallel-port interface is turned into a JTAG programmer to the FPGA. The Xilinx ISE tools can then be used to read-back the FPGA configuriation for example or to even inspect internal signals, using 'ChipScope Pro'.

Clock configuration

The board contains several versatile clock sources. A 16MHz quartz osciallator is connected to the GCK2 (pin 88) input. This clock is always available and can be used to generate several other clocks using the internal clock management resources of the FPGA. When even more clock options are required, an external PLL chip can be used to generate up to three different clocks from this clock source. The CY22393 from Cypress can be programmed using an I2C

interface and contains three independent PLLs. It is capable of generating clock signals up to 200MHz, in par with the capabilities of the FPGA. There is a configuration program available for downloaded from Cypress that can be used to generate configuration files for the PLL chip.

Power

Two linear regulators are used to generate the required voltages for the FPGA and it's supporting circuits for an extrnal power source in the 5-9V range. A feed-back from the FPGA (pin 44) can be used to alter the core voltage of the chip using a PWM modulated signal. This can be used for interesting experiments, however it is important to note that with this feedback it is possible to supply core voltages to the FPGA which it was not designed to handle. While it is not very likely that this will permanently damage the chip, under extreme circumstances it is possible that the core voltage swings over the absolute allowed maximum of 3V. For this reason a jumper (JP_PWR) is put in this feedback path to physically interrupt it and prevent accidental damage to the circuit.

Design files

Schematic and PCB in PDF format (HSNCL)
FPGA downloader with source code (HSNCL)