hcAT91

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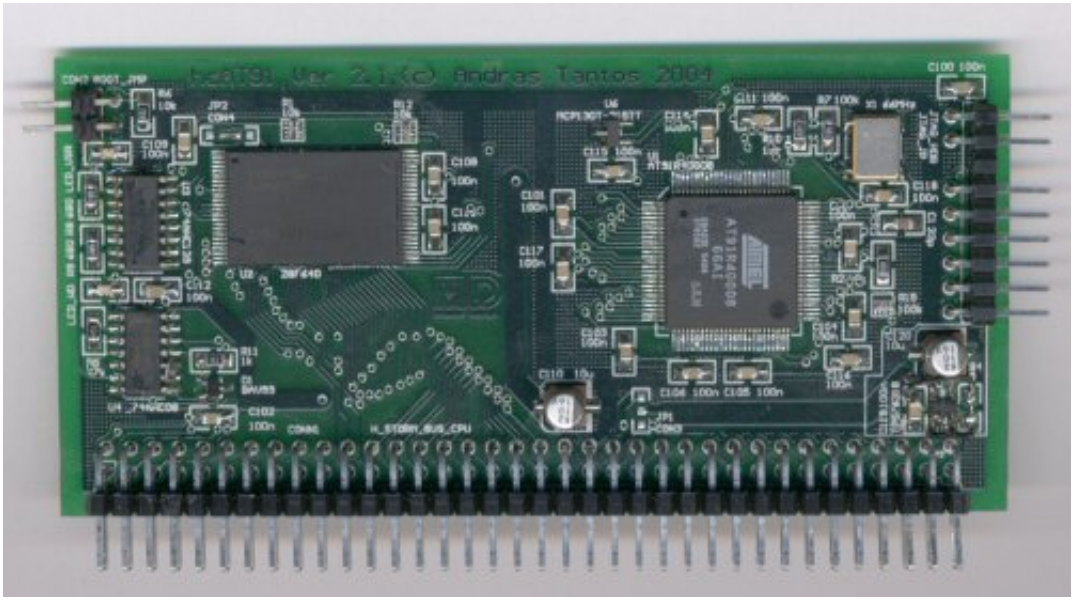

Introduction

This CPU card is built around the ATMEL AT91R40008 microcontroller. That device integrates a 66MHz ARM7TDMI processor core with 256kBytes of on-chip SRAM and a wide set of peripherials. The processor employs a 32-bit internal and a 16-bit external bus architecture.

The CPU card combines this microcontroller with a sizable 16-bit FLASH ROM of up to 8MByte in size, and some support circuitry.

The exceptionally low power-consumption of the ARM processor architecture is even further reduced by the 1.8V core power voltage. This power can be produced on-board by a small LDO regulator or provided externally.

The processor can be programmed in a variety of languages using the GNU toolchain, like C/C++ Pascal or ADA. There are also several other commercial development tools available from many vendors.

Features

- 66MHz ARM7TDMI processor core
- 256kb zero wait-state RAM
- up to 8MBytes of 16-bit FLASH memory
- A user-programmable LED to display program state
- A watch-dog LED that lights up if a watch-dog event occured

- Optional internal core power supply
- 8-bit or 16-bit external bus operations are supported
- versatile bus-interface with programmable speed for each different peripherial slot
- Two serial ports
- Three timer/counters
- up-to 22 digital I/O lines
- JTAG debug interface
- can boot from internal FLASH or from external memory connected to nSEL0
- on-board reset generator

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Design description

CPU

The CPU on the module is the AT91R40008 from Atmel. This microcontroller contains a powerfull 66MHz, 32-bit ARM7TDMI microprocessor, 256kBytes of zero wait-state SRAM memory with a slew of peripherials:

- Three timer/counters
- Up to 6 PWM channels (using the timers)
- Two serial ports, each capable of syncronous and asyncronous operation
- 32 genernal purpose I/O pins (multiplexed with other functions and not all available on the H-Storm connector)
- Flexible interrupt controller
- Watchdog timer

For details, please see the datasheet of the processor at the ATMEL website.

Though the processor employs a 32-bit internal architecture it has only a 16-bit external bus-interface. This interface is used in the hcAT91 CPU card to communicate with the on-board FLASH memory and the other H-Storm devices connected to the H-Storm system bus.

The CPU supports both the 32-bit ARM and the 16-bit THUMB instruction set. While the ARM instruction set provides the best performance when executing from the internal RAM, the THUMB instruction set with its smaller code-size is better suited for code executing directly from FLASH or when code size is a concern.

Since the CPU boots from FLASH memory, all the interrupt vectors are hard-coded in the FLASH. That would prevent user-code to install its own interrupt vectors. To solve this issue, the CPU supports two alternative memory-layouts, switchable through a 'REMAP' command. After this command, the address space around address 0 is mapped to internal SRAM and thus interrupt vectors can be modified. Normally user applications run in this 'canceled REMAP' mode, and at least partitially from internal SRAM.

FLASH memory

The hcAT91 card can accomodate various sizes of FLASH memories from 1 megabit to 64 megabit. Currently a 16 megabit device is standard on the card, giving 2MBytes of storage space.

Upon reset the CPU starts execution at the address 0 of the FLASH memory (unless the card switched to programming mode) so a bottom-boot-block FLASH device was selected.

The memory width of the FLASH memory is 16-bits and the device supports 3V only operation, so programming and erasing the FLASH content can be done by software.

Direct code-execution from FLASH is supported, in fact that's the normal boot-operation of the device: the boot-program executes directly from FLASH. Since this type of memory is significantly slower than the internal SRAM memory, when high-performance is required, code has to be copied into the internal SRAM memory of the CPU and executed from there. Also, with the use of the 'REMAP' function of the CPU interrupt vectors can be mapped to the internal SRAM and thus modified by the executing program.

The FLASH device can be programmed using only software means. To prevent accidental overwrite or erase of the FLASH content however various safety locks are incorporated into the memory. One of these safety locks prevents FLASH programming code to be executed from FLASH as a side-effect. This means that any application that modifies FLASH content has to be at least partially executed from SRAM.

H-Storm bus support

The card supports 8- and 16-bit normal read and write operations. DMA is not supported. Three external address spaces are available (through nSEL0...nSEL2) with highly flexible timing setup. Interface timing can indipendently set for each address space. External wait-state generation is supported. The PROG signal turnes the card into a special programming mode, when after reset it boots from a memory connected to the nSEL0 line instead of the on-board FLASH.

Three external interrupt lines are supported with both edge and level triggering. The nIRQ0 signal is connected to the CPUs FIQ interrupt and thus have shorter latency than the other two signals.

The plug-and-play bus is implemented with two GPIO signals of the CPU.

The two serial ports, the three time channels and a number of GPIO lines are available on the user-defined pins of the connector. Since all the timer and serial port pins can be used as GPIO as well up to 20 GPIO lines are available.

The serial ports are connected to IO group A and B, however they use only four of the available six pins. Both the transmit and the receive clock signals are connected to the same pin of the CPU. Please refer to the schematic or the datasheet for additional information. **IMPORTANT!** The TXD1 line (pin56) doubles as a tri-state enable signal upon hardware reset. This pin has an internal 10k pull-up resistor however make sure not to drive this pin to low when the nRESET signal is active. If this pin is low while the device is reset, all pins of the CPU will be tri-stated and the device will not boot.

Watchdog LED

The CPU card provides visual feedback to the internal watchdog of the CPU card. The LED is turned off by default and is turned on once the watchdog timer signalled. It can only be turned off by a HW reset. This LED provides a simple feedback of the health of the system.

User LED and jumper

An LED is provided on the board that can be controlled from SW, using one of the GPIO lines of the CPU. This LED can be used to provide feedback of the status of the system to the user. For example this LED can be used to provide a 'heart-beat' so that with a quick look it can be determined if an application is executing on the system.

A jumper is also provided on the board whose state can be checked from software. It can be used to modify the operation of the application. For example it can be used to turn on debugging or 'development' code in the application, like logging of events on the serial port.

Reset circuitry

A reset generator IC is mounted on the board. It ensures proper initialization of the CPU and also generates power-on-reset on the nRESET pin of the H-Storm bus.

Power distribution

A optional on-board regulator provides the required 1.8V core power for the CPU. This power is derived from the standard 3.3V power supply that drives all the rest of the components of the system. When this power supply is implemented, the CPU card can operate in a single 3.3V-volt supply environment, with a slightly higher power consumption. When the power supply components are not populated, the CPU card requires two power lines but the power consumption is optimal.

Non H-Storm compatible modes

Though the CPU card was designed to be operated in an H-Storm compatible system, it can operate in other environments as well. If the restrictions on pin-funcitonality of the H-Storm connector is lifted some interesting operating modes can be used.

- Since the plug-and-play interface lines (Pin 71 and 72) are implemented with GPIO lines of the CPU, those signals can be used as two additional digital I/O lines.
- The nSEL1, nSEL2 nIRQ0..2 signals (pin 6...10) can double as GPIO lines. If the original function of those pins is not required, they can be used as 5 additional I/O lines.
- The IOD3 signal (pin 66) can be used as an additional interrupt source

With all these, the maximum number of I/O lines available on the module can be increased to 27. Note however, that some of these lines contain internal pull-up resistors so consult the

schematic of the module before using these pins in this alternate mode.

In-circuit emulation support

The hcAT91 cpu card supports the embedded in-circuit emulator module in the CPU. This emulation module uses the JTAG interface. All of its signals are connected to a standard H-Storm in-circuit emulator connector. A cheap emulator HW, like the Wiggler in conjunction with GDB can be used to download and debug programs on the HW.

Power consumption

The CPU consumes in the range of 55mW under normal operating circumstances. In a single-supply scennario that would lead to an around 100mW total power consumption or about 33mA of supply current. When idleing the power requirement drops to around 1/10th of the operating current that is, to 3mA.

Design files

User's manual for the hcAT91 CPU card in PDF format (HSNCL)
Schematic and PCB in PDF format (HSNCL)