hcPCI

Author : Andras Tantos

Introduction

This CPU card quite special in the H-Storm product family. It is a PCI 2.2 compatible 32-bit PCI card that converts any regular PC into a full-featured H-Storm CPU card.

The card is designed around the PLX PCI9030 target PCI interface chip. It provides a simple and easy to use interface to any PC with a PCI connector.

The card can be used for two purposes.

- It can be used as a PCI to local bus interface to a add custom peripherals to a PC without the hassle of dealing with the PCI bus
- It can be used a standard H-Storm CPU module and interface a PC to an existing H-Storm system.

Features

- 32-bit, 33MHz PCI 2.2 compliant 3.3V PCI interface
- PLX PCI9030 PCI target interface chip
- 16-bit local-bus interface
- Syncronous or asyncronous operation on the local-bus side
- Up to 60MHz operation on the local-bus side
- Four independently programmable chip-selects with flexible wait-state generation
- 8MB (4MWord) of address-space for each chip-select

- Three interrupt and three DMA sources, routed to a single PCI interrupt line
- H-Storm compatible DMA operations is possible through emulation
- 3.3V power supply for local-bus peripherals with optional 2.5V and 1.8V regulators
- Four 16MByte address spaces are allocated from the PC address space
- Fully compatible with the H-Storm compact connector specification

License

This document and all the accompanying design documentation (for example schematic and PCB files) are covered by the H-Storm Non-Commercial License (HSNCL).

H-Storm Non-Commercial License (HSNCL)

Redistribution and use in source or binary forms, or incorporated into a physical (hardware) product, with or without modification, are permitted **for non-commercial use only**, provided that the following conditions are met:

- **The redistribution doesn't result in financial gain.**
- Redistributions of source code must retain the above copyright notice, this list of conditions and the following disclaimer.
- Redistributions in any other form must contain in printed or electronical format the above copyright notice, this list of conditions and the following disclaimer in the documentation and/or other materials provided with the distribution.
- All advertising materials mentioning features or use of this technology must display the following acknowledgment:
  This product includes H-Storm technology developed by Andras Tantos and Modular Circuits.
- Neither the name of Andras Tantos or Modular Circuits may be used to endorse or promote products derived from or using this technology without specific prior written permission.

ALL THE INFORMATION, TECHNOLOGY, AND SOFTWARE IS PROVIDED BY THE AUTHORS ``AS IS'' AND ANY EXPRESS OR IMPLIED WARRANTIES, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE ARE DISCLAIMED. IN NO EVENT SHALL ANDRAS TANTOS, MODULAR CIRCUITS OR CONTRIBUTORS BE LIABLE FOR ANY DIRECT, INDIRECT, INCIDENTAL, SPECIAL, EXEMPLARY, OR CONSEQUENTIAL DAMAGES (INCLUDING, BUT NOT LIMITED TO, PROCUREMENT OF SUBSTITUTE GOODS OR SERVICES; LOSS OF USE, DATA, OR PROFITS; OR BUSINESS INTERRUPTION) HOWEVER CAUSED AND ON ANY THEORY OF LIABILITY, WHETHER IN CONTRACT, STRICT LIABILITY, OR TORT (INCLUDING NEGLIGENCE OR OTHERWISE) ARISING IN ANY WAY OUT OF THE USE OF THIS SOFTWARE OR TECHNOLOGY, EVEN IF ADVISED OF THE POSSIBILITY OF SUCH DAMAGE.

Design description

PCI to local-bus interface

The card sports a PLX PCI9030 target PCI interface chip. This is a flexible PCI to local bus interface chip. The device supports 33MHz host PCI-bus operation with up to 60MHz of local-bus clock. The card uses the 33MHz PCI clock to run the local-bus side with an optional local-bus clock generator for even faster operations. The card supports only 16-bit local-bus operations in accordance with the H-Storm bus specification even thought the interface chip has support for 32-bit local-bus operation as well.

The interface chip is fully 5V-tolerant on both the local-bus and the PCI-bus side however it uses 3.3V signaling. The PCI interface is compliant to the PCI 2.2 specification.

Serial EEPROM

The PCI9030 chip loads its configuration from an exnternal serial EEPROM device upon powerup and defaults to a standard configuration if the memory chip is not detected. The hcPCI card contains an external EEPROM chip however the data-out line to the PLX chip can be interrupted by a jumper. It is possible to configure the EEPROM in such a way that the PLX chip will not work correctly if that configuration is read back from the memory even to the point where the entire system would not boot. In such case, the jumper can be removed. When the jumper is removed the PLX chip will not detect the serial configuration ROM upon the next powerup, and will load its default configuration. When the system is booted up, the jumper can be put back to its place so that the content of the EEPROM can be corrected. This jumper is called JP_EEPROM and should not be removed under normal circumstances.

This EEPROM device not only contains the power-up configuration of the defice but potentially can be used to store additional data, called the VPD information. The card is fully compliant to the VPD specification. See the PCI 2.2 standard or the PCI9030 chip datasheet for details.

H-Storm bus interface

The local-bus interface on the card is fully compliant to the H-Storm bus specification. The connector is a compact extended H-Storm bus connector which means that the signals for the bus-extension connector are brought out to the card-specific pins of the standard connector. This provides full compatibility with the standard H-Storm bus specification, while adds support for the extended address range and DMA capabilities of the extended H-Storm bus connector. A simple passive converter can be designed that converts this compact connector to an extended H-Storm bus connector. The card provides an 8MB (4 MWord) address range for each of the three perihperal-select signals (nSEL0..3).

The card supports 8- and 16-bit normal and burst read and write operations. DMA is supported through emulation. Three external address spaces are available (through nSEL0...nSEL2) with highly flexible timing setup. Interface timing can indipendently set for each address space.

External wait-state generation is supported. The PROG signal is not connected.

Interrupts are routed to the PCI interface INTA pin. These interrupts can be edge or level-sensitive and active high- or low-level though the current CPLD configuration supports active-low level-sensitive interrupts only.

DMA requests (nDRQ0..3) are also converted to interrupt requests on the PCI interface INTA pin. The card being a target-only device cannot take ownership of the PCI bus and initiate transfers on its own. H-Storm DMA cycles can be emulated in the interrupt service routine. The nDACK line is connected to the (inverted) A22 pin of the local bus. This means that every access to the local bus where the address is in the lower 8MB is treated as a normal bus operation while accesses to the higher 8MB of address space is seen as a DMA cycle. For each peripheral select signal a full 16MB address space is allocated on the PCI bus to accomodate for both normal and emulated DMA operations.

The plug-and-play bus of the H-Storm connector is connected to two GPIO signals of the PCI9030 chip. Software-based I2C communication can be used to access the PnP bus. GPIO0 is connected to the PnP_D while GPIO1 to the PnP_C lines.

The PCI9030 chip has two interrupt source inputs. IRQ1 is asserted if any of the H-Storm bus IRQ pins (nIRQ0..2) is low, while IRQ2 is used to request DMA operations in the same way. Three GPIO lines can be used to find out which of the three possible sources on each line is active while a fourth GPIO line is used to select between IRQ and DRQ sources. The logic is as follows:

	if GPIO8 is '0'	if GPIO8 is '1'
than GPIO4 is	nIRQ0	nDRQ0
than GPIO5 is	nIRQ1	nDRQ1
than GPIO6 is	nIRQ2	nDRQ2

GPIO7 is used to enable this operation: if GPIO is set to '0', GPIO4..6 is turned off and floated.

Additional local-bus functionality

The card also provides some additional functionality to be used with non-H-Storm compatible designs. These are:

- A fourth peripheral-select signal (nSEL4) is driven out to pin A65. It is functionally equivavlent to nSEL0..3
- The local clock (LCLK) is driven out to pin A68 for synchronous local-bus operations
- Additional local-bus masters can gain control over the local-bus by requesting access on the LREQ (A67) line and give access by the LGNT (A66) line.

Power

The card uses the PCI connector to derive its power. It contains a 3.3V regulator that can be used to power devices on the H-Storm bus. If that is not required the power supply towards the H-Storm connector can be interrupted by a jumper.

Optional 2.5V and 1.8V power supplys are also available on the board that can be used to provide all the possible power lines for an H-Storm device.

Reset circuitry

The CPU card generates the nRESET signal but does not respond to external reset pulses from the H-Storm bus.

Design files

Schematic and PCB in PDF format (HSNCL)
CPLD configuration sources (HSNCL)
Default EEPROM configuration and download utility (HSNCL)