hpCS8900

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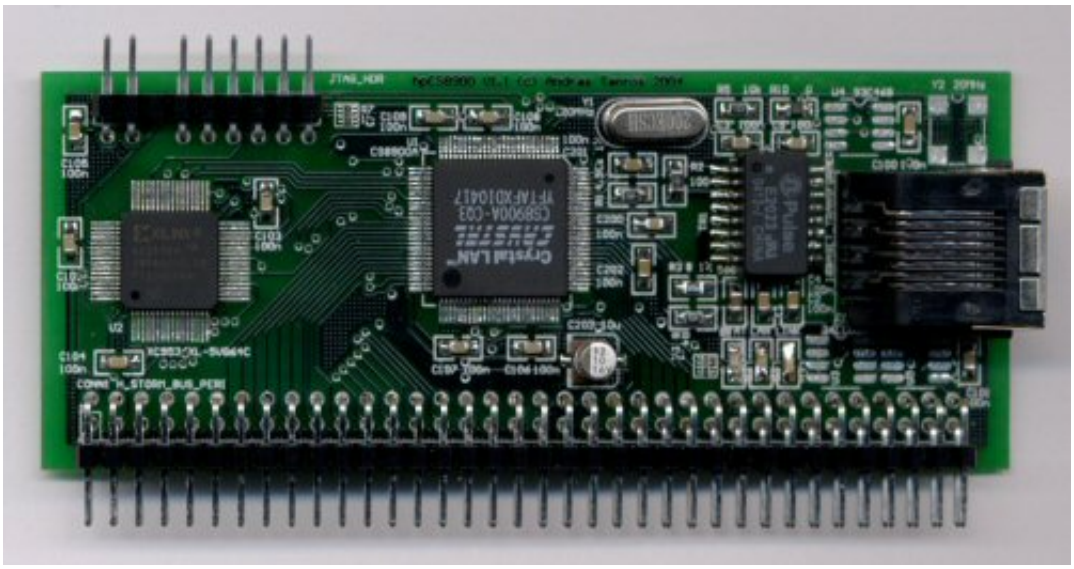

Introduction

This peripheral module adds Ethernet connection capabilities to an H-Storm compatible system. It uses the CS8900 10Mbit Ethernet chip from Cirrus Logic as the main interface component. The card also contains the required support electronics to connect to a 10BaseT (UTP) network and some digital interface logic to interface the Ethernet controller chip to the H-Storm bus.

The card support 10Mbit of transfer rate in each direction, using a full duplex connection. This doubles the maximum available data rate to 20Mbit per second. The card operates form a single 3.3V power supply.

Features

- 10MBit Ethernet support with full duplex capability
- 10BaseT connector on board
- Three status LEDs on board
- AUI interface signals are available on the H-Storm connector (interface transformer has to be provided externally)
- 16-bit bus interface
- Indexed packet-page interface
- Optional direct packet-page interface
- DMA operation is **not** supported as the basic H-Storm connector doesn't have such resources
- Generates external wait-states

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Design description

The Ethernet chip

The network interface chip used on this peripheral module is the CS8900 from Cirrus Logic. The

board uses the 3.3V version of the IC. This device is a single chip 10Mbit ethernet interface that incorporates both the MAC and the PHY layers of the Ethernet network stack. It was originally designed for the ISA bus of the PC architecture but now it is one of the most popular embedded ethernet chips on the market.

The chip has direct support (through interface transformers) for 10BaseT (UTP) and AUI interfaces. The card contains the support electronics and the interface transformer for the 10BaseT interface while it provides all the connections necessary to implement an AUI interface externally.

The chip supports both 16- and 8-bit operations, though the interrupt generation function is not operational in 8-bit mode. The card supports 16-bit operation of the chip only. The chip generates wait-states to make the bus-cycles long enough. The bus-cycles must be at least 157ns long so CPU cards that cannot generate long enough access cycles must support external wait-state generation to interface with this module.

The chip supports 4 interrupt lines though only one of the IRQ lines (IRQ0) is connected on the module to the nIRQ0 line.

DMA operation that is supported by the chip is not available on the module: the standard H-Storm bus connector doesn't have support for DMA operations.

The boot-ROM support of the IC is not supported on the module. The configuration EEPROM is optional and can be mounted on the module. The module however is fully functional without that configuration chip provided the CPU module configures the module after powerup.

The Ethernet chip supports indexed and direct access to its internal packetpage memory. The module currently provides support for only indexed access with direct access available as a downloadable CPLD upgrade latter.

Support electronics

The Ethernet chip is interfaced to the H-Storm bus with a Xilinx XC9536XL CPLD. This provides easy upgrade and full support for all the required interface needs in a fast signle chip implementation.

The analog interface with the interface transformer along with an RJ45 connector is provided on board for 10BaseT Ethernet connections. The digital interface signals for an AUI interface is available on the user-defined part of the H-Storm connector. The signals for the 10BaseT interface are not available on the H-Storm connector for EMI reasons.

Three status LEDs are integrated on board: LINK, STAT and LAN. The signals driving these LEDs are also available on the H-Storm connector if external monitoring of these signals is needed.

Power requirements

The module is powered by a single 3.3V power supply. The power maximum power consumption of the module is less than 100mA.

H-Storm bus support

The hpCS8900 peripheral module is fully compatible with the H-Storm standard module specification. It supports 16-bit operations only. It does not support burst read and write operations, and generates external wait-states. It uses a single module-select signal (nSEL0) and generates interrupts on a single interrupt line (nIRQ0). The module only generates LVTTL3-compatible signals on the user-defined part of the H-Storm bus. It drives a total of 9 user-defined lines. It has no user-defined inputs.

The reset signal pulse (nRESET) must be at least 400ns wide. The bus-cycles must be at least 157ns long if no external wait-states are supported. The nWait line is assarted in less than 42ns after an active cycle is recognized.

The module presents a single CMOS gate load on all but the D0..D7 lines. On the lower 8-bits of the data-bus it presents a two CMOS gate load.

Design files

Schematic and PCB in PDF format (HSNCL)